REMARKS

The Office Action dated April 16, 2004, has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1, 8, 28 and 57 have been amended to correct informalities. No new matter has been added. Further, the amended claims are entitled to their full range of equivalents because the amendments were not made to overcome a statutory rejection. The amendments were made merely to correct informalities. Thus, claims 1-60 are presently pending and are respectfully submitted for consideration.

Claims 1, 8 and 57 were objected to because of informalities. Applicants amend claims 1, 8 and 57 to correct the informalities. Thus, the objections are rendered moot.

Claims 1-60 were rejected under 35 U.S.C. §03(a) as allegedly being unpatentable over U.S. Patent No. 6,021,132 (*Muller et al.*) in view of U.S. Patent No. 6,529,519 (*Steiner et al.*) The Office Action took the position that *Muller* disclosed all the elements of the claimed invention, with the exception of "a single buffer for packet mechanism." *Steiner* was cited as curing the deficiencies in *Muller*, and the Office Action alleged that it would have been obvious to a person of ordinary skill in the art to combine *Muller* and *Steiner* to yield the claimed invention. Applicants respectfully submit that the presently pending claims recite subject matter that is neither disclosed nor suggested in the cited references.

Claim 1, upon which claims 2-7 are dependent, recites a memory structure. The memory structure includes an Address Resolution Table for resolving addresses in a packet-based network switch. The memory structure also includes a Packet Storage Table, the Packet Storage Table adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted.

Claim 8, upon which claims 9-12 are dependent, recites a memory structure comprising an Address Resolution Table having an associative memory structure. The Address Resolution Table resolves addresses in a packet-based network switch. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted.

Claim 13, upon which claims 14-27 are dependent, recites a memory structure having a memory block. The memory structure includes an Address Resolution Table having an associative memory structure. The Address Resolution Table resolves addresses in a packet-based network switch. The memory structure also includes a Transmit Descriptor Table. The Transmit Descriptor Table is associated with a

corresponding packet-based network transmit port, and the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value. The memory structure also includes a Packet Storage Table. The Packet Storage Table is adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted.

Claim 28, upon which claims 29-31 are dependent, recites a packet-based switch comprising a shared memory structure having an Address Resolution Table and a Packet Storage Table. The packet-based switch also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted.

Independent claims 32, 52 and 57 recite subject matter similar to the claims disclosed above.

As discussed in the specification, the present invention enables a memory structure to resolve addresses in a packet-based network switch. The present invention enables bandwidth savings that can be attributed to a one buffer-per-packet approach. The single buffer-per-packet approach enhances the feasibility of a bit-per-buffer pool tracking technique and the need to search a larger buffer structure can be mitigated or eliminated.

It is respectfully submitted that the cited references of *Muller* and *Steiner*, when viewed alone or combined, fail to disclose or suggest the elements of the presently pending claims. Therefore, the prior art fails to provide the critical and unobvious advantages discussed above.

Muller relates to shared memory management in a switch network element. *Muller* describes a shared memory manager for a packet forwarding device that includes a pointer memory having stored information regarding buffer usage for each of a number of buffers in a shared memory. *Muller* also describes an encoder that is coupled to the pointer memory for generating an output that indicates a set of buffers that contains a free buffer. The shared memory manager includes a pointer generator for locating a free buffer in the set of buffers. *Muller* describes the pointer generator producing a pointer to the free buffer based upon the output of the encoder in the location of the free buffer within the set of buffers.

Steiner relates to prioritized-buffer management for fixed size packets in a multimedia application. *Steiner* describes a memory system that includes a tag register for storing tags associated with respective pages, wherein each tag indicates whether the associated page is empty or full. *Steiner* also describes a shadow register for storing conflict-free updates from the tag register and a page register for storing pointers to the lowest free or unoccupied page. *Steiner* also describes a buffer that is organized along packet boundaries or pages for convenience of operation. A processor, or MPU 34, maintains a table of pointers to each packet boundary, and, therefore, knows the location

of all leftover packets. A tag register 40 is provided, that has as many bits as there are packet boundaries of buffer 22. *Steiner* describes buffer 22 being implemented as a dual port ramp, with one port being randomly accessed by MPU 34 while the other port is sequentially accessed by an address or byte counter 42.

To establish obviousness, the cited references must disclose or suggest all the features of the claimed invention. Applicants submit that neither *Muller* nor *Steiner*, either alone or in combination, discloses or suggests all the features of the presently pending claims. For example, applicants submit that the cited references do not disclose a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted.

In contrast, the present invention discloses "a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted," as recited, for example, in claim 1. This feature also is recited in the subject matter of the other pending independent claims. Applicants respectfully submit that the cited references do not disclose or suggest at least this feature of the pending claims.

The Office Action states that *Steiner* yields "a buffer with reduced processor loading and increased power-conservation." Referring to *Steiner*, Figure 3 shows a prioritized buffer 22 and a tag register 40 that has as many bits as the number of packet

boundaries in buffer 22. Buffer 22 is composed of dual port memories in which scheduling takes place. Stream data enters buffer 22 via its sequential port to be operated on via its RAM port by MPU 34. Thus, applicants submit that *Steiner* describes a single buffer that receives packets.

According to the claimed invention, a single buffer per packet mechanism configured to receive an individual packet is disclosed. Applicants submit that the embodiments recited in the claims are not limited to a single buffer for all packets. The claimed invention is not limited to a single buffer, but a single buffer per packet mechanism. Applicants further submit that *Steiner* does not disclose or suggest this feature and, therefore, does not provide those limitations of the claimed invention missing from *Muller*.

As discussed in the specification on page 7, lines 9-29, one transmit descriptor read per packet is performed with one buffer per packet, thereby eliminating multiple memory accesses to find a linked list of buffers. One access is executed in order to locate the entire packet to be transmitted. In a linked-list buffer approach like *Steiner*, a fixed buffer block size is employed that requires additional transmit descriptor reads to locate each subsequent block that causes a reduction in bandwidth. Thus, the claimed features are distinguishable from *Steiner*.

Applicants also note that the Office Action cites passages within *Steiner* that describe problems within the art as resolving memory fragmentation problems while conserving processor resources. It is unclear to applicants how problems within the prior

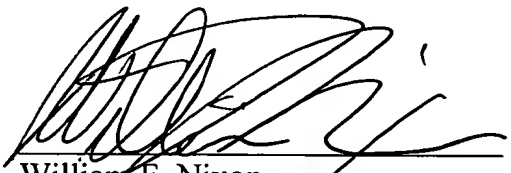
art are able to solve, disclose or suggest the features of the present invention. Further, applicants submit that listing problems known in the art does not solve or teach solutions to these problems. Thus, applicants maintain that *Steiner* does not disclose or suggest those features of the claims missing from *Muller*.

It is respectfully submitted that no combination of *Muller* and/or *Steiner* discloses or suggests the subject matter of the presently pending claims. It is further submitted that each of claims 1-60 recites subject matter that is neither disclosed nor suggested in the cited references. It is therefore respectfully requested that all of claims 1-60 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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